Key Sheet
AD7792/AD7793

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Highlights of the AD7792/AD7793—3-Channel, Low Noise, Low Power, 16-/24-Bit Sigma-Delta ADCs with On-Chip In-Amp and Reference

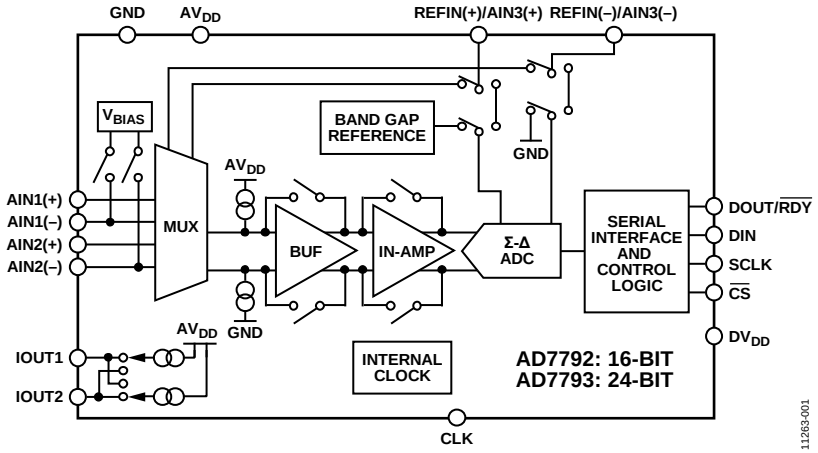

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

This key sheet[1] provides users with an overview of the AD7792/AD7793. Key attributes of the parts include the following:

- Designed for the measurement of wide dynamic range, low frequency signals, such as those in thermocouple and resistance temperature detector (RTD) measurements, gas analysis, industrial process control, blood analysis, and portable instrumentation.
- Low power, flexible, high performance, low noise, 16-/24-bit sigma-delta (Σ-Δ) ADC suitable for converting low input bandwidth analog signals with a fully flexible output data rate (ODR) between 4.17 SPS and 470 SPS.
- An on-chip low noise instrumentation amplifier allows signals of small amplitude to interface directly to the ADC.
- Combines three differential input channels with low power consumption.
- With an ODR of 4.17 SPS and a gain of 64, the AD7792/AD7793 boast an rms noise of 40 nV.
- Contains a precision low noise, low drift internal band gap reference and can accept an external differential reference.
- Available in a 16-lead TSSOP package, allowing a reduced board size.

FEATURES AND BENEFITS

The AD7792/AD7793 offer the following features and benefits:

- Simultaneous 50 Hz and 60 Hz rejection at 16.7 SPS ODR
- Programmable gains of 1, 2, 4, 8, 16, 32, 64, and 128
- Internal and system calibration on chip
- Option of 64 kHz internal clock or external clock
- Ultralow noise performance across the ODR range
- Fully compatible with SPI, QSPI™, MICROWIRE®, and DSP
- SPI configuration control
- 3-wire serial digital interface (Schmitt trigger on SCLK)

[1] This document provides users with an overview of the AD7792/AD7793; it is not a notice of performance or intent. Refer to the AD7792/AD7793 data sheet for performance and more specific information about these products.

Rev. 0

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KEY CHARACTERISTICS

FUNDAMENTAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
ADC Type		Σ-Δ ADC		
Number of Input Channels		Three differential input channels		
Resolution				
AD7792	16		16	Bits
AD7793	24		24	Bits
Output Data Rate (ODR)	4.17		470	SPS
Differential Input Voltage Range	$-V_{REF}$/gain		$+V_{REF}$/gain	V
Power Supply Voltage				
AV_{DD} with Respect to GND	2.7		5.25	V
DV_{DD} with Respect to GND	2.7		5.25	V
Power Supply Current (I_{DD})				
With External Reference (AV_{DD} = 3 V, Buffer Off)		110		μA
With Internal Reference (AV_{DD} = 3 V, Gain = 4 to 128)		400		μA
Offset Error		±1		μV
Offset Error Drift vs. Temperature[1]		±10		nV/°C
Full-Scale Error		±10		μV
Gain Drift vs. Temperature (Gain = 1 to 16, External Reference)		±1		ppm/°C
Integral Nonlinearity (INL)	−15		+15	ppm of FSR
Power Supply Rejection	100			dB
Operating Temperature Range	−40		+105	°C

[1] Recalibration at any temperature removes these errors.

NOISE

Table 2. RMS Noise (nV) vs. Gain and Output Data Rate Using an External 2.5 V Reference

	RMS Noise (nV)							
Output Data Rate (SPS)	G = 1	G = 2	G = 4	G = 8	G = 16	G = 32	G = 64	G = 128
4.17	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.2	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
123	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
242	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
470	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

OPERATING THE AD7792/AD7793

DATA INTERFACE

The data interface for the AD7792/AD7793 is

- Performed using a 4- or 3-wire SPI
- Compatible with SPI, QSPI, MICROWIRE, and DSP
- Allows a user to both write to and read from the AD7792/AD7793 on the same data bus
- Indicates when transferred data is available by bringing the DOUT/$\overline{RDY}$ signal and the $\overline{RDY}$ bit in the status register low

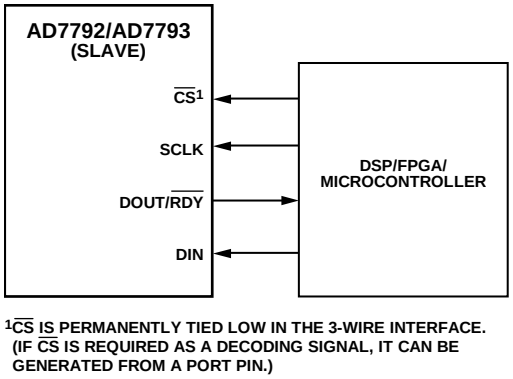

Figure 2. AD7792/AD7793 Data Interface, 4-Wire SPI

Table 3. 4-Wire Serial Interface Pin Functions

Pin	Function
$\overline{CS}$[1]	Selects the ADC (also applicable in systems with multiple devices on the serial bus).
	Provides a frame synchronization signal.[2]
SCLK	Determines when data transfers (either on DIN or DOUT/$\overline{RDY}$) occur.
DOUT/$\overline{RDY}$	Accesses data from the on-chip registers.
	Indicates when the transferred data is available.
DIN	Transfers data into the on-chip registers.

[1] $\overline{CS}$ is permanently tied low in the 3-wire interface. (If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin.)

[2] Useful for DSP interfaces. The first bit (MSB) is effectively clocked out by $\overline{CS}$ because $\overline{CS}$ typically occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

DATA MODES

There are three data modes available: continuous conversion mode, continuous read mode, and single conversion mode.

Continuous Conversion Mode (Default)

Continuous conversion is the default power-up mode. In this mode, the AD7792/AD7793 convert continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required.

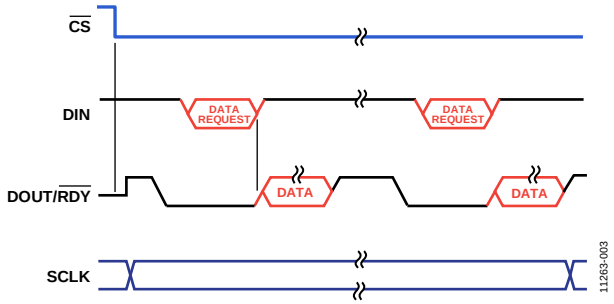

Figure 3. Continuous Conversion Mode

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7792/AD7793 can be configured so that the conversions are automatically placed on the DOUT/$\overline{RDY}$ line. By writing 01011100 to the communications register, the user need only apply the appropriate number of SCLK cycles to the ADC, and the conversion word is automatically placed on the DOUT/$\overline{RDY}$ line when a conversion is complete.

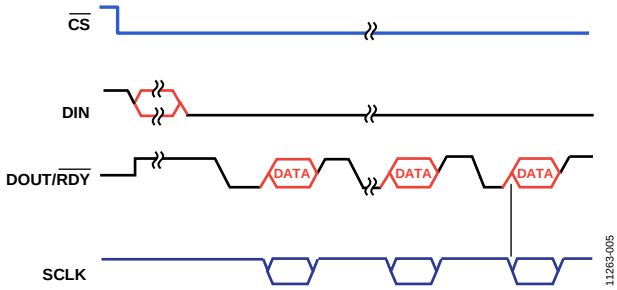

Figure 4. Continuous Read Mode

When DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC. The data conversion is then placed on the DOUT/$\overline{RDY}$ line. When the conversion is read, DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once.

In continuous read mode, the serial interface is dedicated to reads of the data register. If any other register needs to be accessed, continuous read mode must be disabled. In addition, every time a conversion is available, the serial interface is reset in this mode. Therefore, it is essential that the conversion be read before the next conversion is available.

While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

Single Conversion Mode

In single conversion mode, the AD7792/AD7793 perform a single conversion and are placed in standby mode after the conversion is complete. DOUT/$\overline{\text{RDY}}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{\text{RDY}}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{\text{RDY}}$ has gone high.

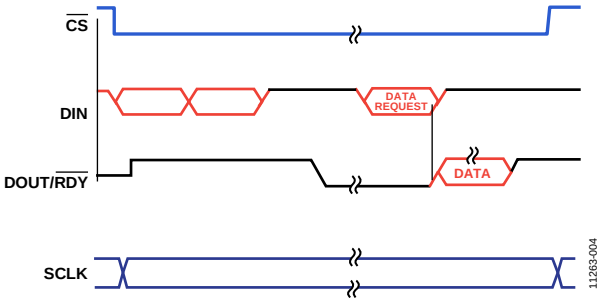

Figure 5. Single Conversion Mode

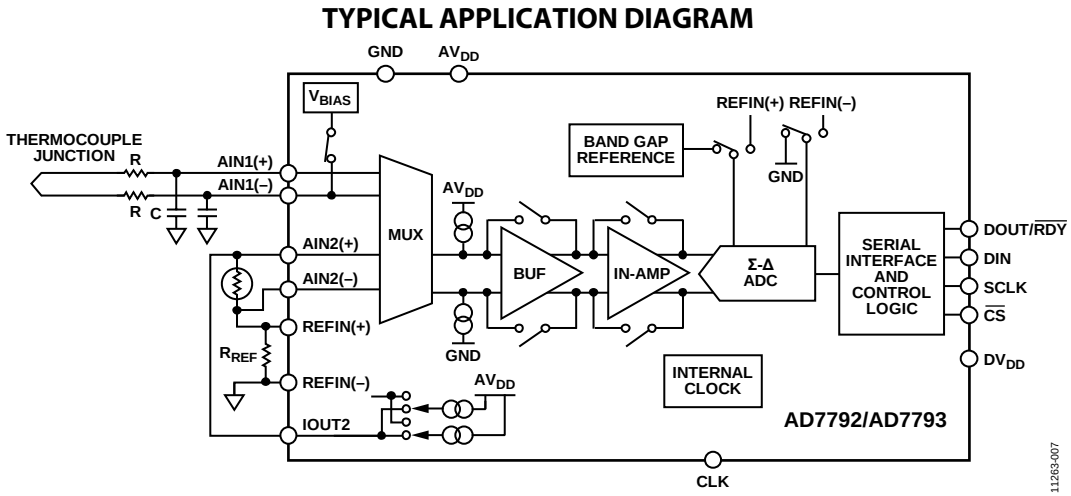

Figure 6. Typical Application Diagram for Thermocouple Measurement

FREQUENTLY ASKED QUESTIONS

What is the optional internal buffer?
The multiplexed input channels of the AD7792/AD7793 are

- Connected to the on-chip buffer amplifier when either device is operated in buffered mode or when the gain is greater than 2
- Connected directly to the modulator when either device is operated in unbuffered mode at a gain of 1 or 2.

In buffered mode, the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant ranges of source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

What digital filter options are available?
The AD7792/AD7793 use slightly different filter types, depending on the output data rate (ODR), to optimize the rejection of quantization noise and device noise. When the ODR is from 4.17 SPS to 12.5 SPS, a Sinc3 filter along with an averaging filter is used. When the ODR is from 16.7 SPS to 39 SPS, a modified Sinc3 filter is used. This filter provides simultaneous 50 Hz and 60 Hz rejection when the ODR equals 16.7 SPS. A Sinc4 filter is used when the ODR is from 50 SPS to 242 SPS. Finally, an integrate only filter is used when the ODR equals 470 SPS.

What is 50 Hz and 60 Hz rejection?
The mains power supply generates interference at 50 Hz or 60 Hz, with the frequency varying from one country to another. The AD7792/AD7793 have the ability to simultaneously reject 50 Hz and 60 Hz signals. Simultaneous 50 Hz and 60 Hz rejection is obtained when the ODR is set to 16.7 SPS.

How do I interface with the part?
The part can be configured by using a 4-wire SPI interface; this interface is also used as the data interface. The SPI interface allows the user to read the status of the part and to change the setup.

Are there any ESD protection schemes that should be considered for the AD7792/AD7793?
These converters are manufactured on a standard CMOS process; therefore, all standard practices and protection schemes that apply to other CMOS devices also apply to these devices. There are ESD protection diodes on all the inputs that protect the device from possible ESD damage due to handling and production. To determine the appropriate ESD precautions, refer to the AD7792/AD7793 data sheet for information about the absolute maximum ratings.

Is an antialiasing filter required?
The analog input is sampled at 128 kHz (that is, on each edge of the master clock). The digital filter does not provide any rejection at this frequency or at frequencies that are multiples of 128 kHz; an external antialiasing filter is required to provide rejection at these frequencies, with a simple RC filter being sufficient. Typical values for the filter are

- 1 kΩ resistor in series with each analog input
- 0.1 μF capacitor between the analog input pins
- 0.01 μF capacitor from each input pin to ground

These typical values can be used only when the buffer is enabled. When the buffer is disabled, smaller RC values are required because larger values can cause gain errors.

Can filtering be added to the reference pins?
The reference input to the AD7792/AD7793 is not buffered. Therefore, the filtering must be limited on the reference pins because large RC values can cause gain errors. The AD7792/AD7793 data sheet lists acceptable RC values for use when the analog inputs are unbuffered. Similar values should be used on the reference pins.

What is the instrumentation amplifier?
Amplifying the analog input signal by a gain of 1 or 2 is performed in the modulator. However, when the gain equals 4 or higher, the output from the buffer is applied to the input of the on-chip instrumentation amplifier. This low noise in-amp means that signals of small amplitude can be gained within the AD7792/AD7793 while still maintaining excellent noise performance.

What calibration options are available?
The AD7792/AD7793 provide four calibration modes that can be programmed via the mode bits in the mode register: internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration, and system full-scale calibration, which effectively reduces the offset error and full-scale error to the order of the noise. After each conversion, the ADC con-version result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

LEARN MORE AND START DESIGNING

To learn more about the AD7792/AD7793 and compatible products or to sample and buy the AD7792/AD7793 devices, click on the links provided or contact an Analog Devices, Inc., sales representative.

COMPATIBLE DEVICES

Table 4. Recommended Compatible Devices[1]

Linear Regulators	Precision References	ADC Driver Amplifiers	Circuits from the Lab™	Evaluation Board
ADP3303 family ADP3330 family	ADR380 family ADR361 family	N/A (the AD7792/AD7793 include an on-board internal buffer)	CN-0206, *Complete Type T Thermocouple Measurement System with Cold Junction Compensation*	AD7792/AD7793 evaluation board

[1] Information about additional companion products are provided on the AD7792 and AD7793 product pages.

PACKAGE DIAGRAM

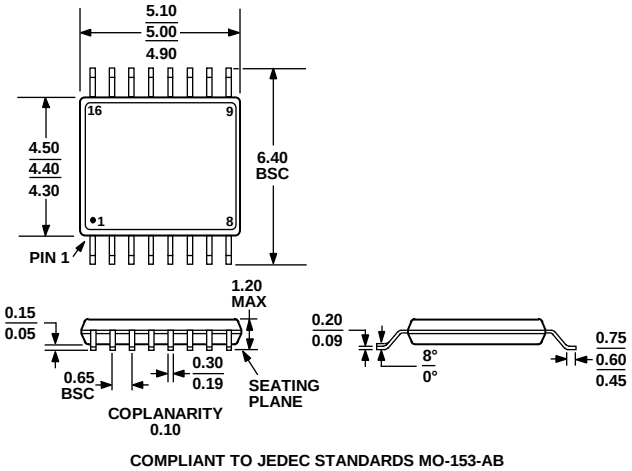

Figure 7. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters

GETTING STARTED

AD7792/AD7793 DATA SHEET

SAMPLE AND BUY THE AD7792

SAMPLE AND BUY THE AD7793

UG11263-0-1/13(0)

ANALOG DEVICES

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